CMOS LAYOUT AND BIAS OPTIMIZATION FOR RF IC DESIGN APPLICATIONS

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ABSTRACT

High frequency and low noise performance of 0.8 μm polysilicon gate CMOS device has been analyzed intensively with the various multi-finger polysilicon gate layout and bias to find the optimal condition. From the analysis, the optimal width of unit gate finger and bias condition have been found to maximize f_{max} and minimize F_{min}. At the conditions, F_{min}, gain and noise resistance characteristics of large width transistors are also analyzed.

INTRODUCTION

CMOS technology has recently been recognized as a good choice for the fabrication of wireless communication system. To integrate baseband, IF and RF modules in a single chip for low cost, BiCMOS or CMOS(SOI) technology is known to be a good candidate. For the RF applications, some works about RF performance of CMOS device have also been published [1],[2], but optimum transistor layout and bias condition for high frequency and low noise operation are not analyzed in detail.

The purpose of this paper is to find out the optimum transistor layout and operating bias condition of 0.8 μm polysilicon gate CMOS for maximizing the RF performance regarding f_{max} and noise.

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MEASUREMENT

CMOS devices used in this work were fabricated using a 0.8 μm twin well CMOS process on silicon wafers with the resistivity of 2000 Ω.cm. For layout optimization, single and multi-finger type nMOSFETs were laid-out with common-source configuration. S-parameter measurements were carried out in the frequency range of 0.5~39.5 GHz using on-wafer RF probes and a HP8510C Network Analyzer. Noise figures were also measured at the frequency of 0.3~3 GHz range using an ATN setup.

RESULTS AND DISCUSSION

1) Gate Geometry Effect on f_{max}

The value of f_{max} for FET can be expressed as follows [3]:

$$f_{max} = \frac{f_T}{2\sqrt{2\pi f_T R_g C_{gd} + G_{ds} R_{in}}} \quad (1)$$

where C_{gd} is the drain to gate capacitance, G_{ds} is the output conductance, and R_{in} is the input resistance consisting of gate, source and channel component. The gate resistance (R_g) is a dominant parameter governing f_{max} with the layout variation of the gate finger in MOSFETs. R_g can be expressed simply as $R_g = R_{\square}\, W/(n^2 L)$, where $R_{\square}$ is the polysilicon sheet resistance, L is the gate length, W is the total gate width, and n is the number of gate fingers.

The scalability of small-signal linear para-

meters of MOSFET, which has been well studied in MESFET [4], can also be applied for MOSFET. For the fixed unit finger width (W_U), two times increase of n leads to two-fold R_g reduction and two-fold increase of C_{gd} and G_{ds}, thus resulting in no variation of f_{max} to the number of finger as shown in Fig. 1. At the fixed W, two times decrease of W_U produces four-fold R_g reduction, in turn yielding $\sqrt{2}$ times increase of f_{max} as shown in Fig. 2.

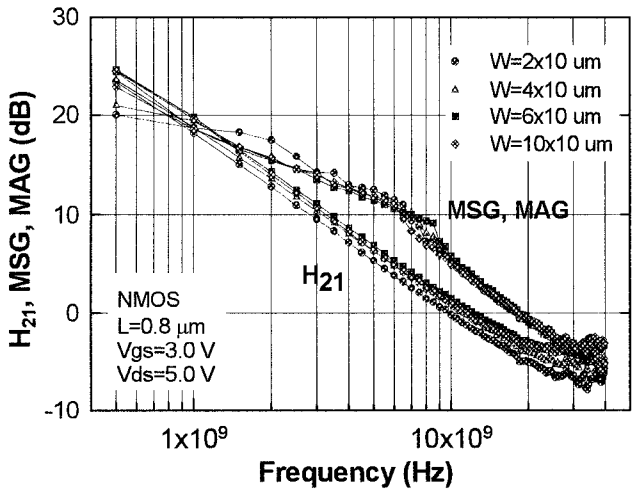

Fig. 1. Measured H_{21} and MAG for 0.8 μm multi-finger nMOSFETs. (2, 4, 6, and 10 fingers, Unit finger width=10 μm)

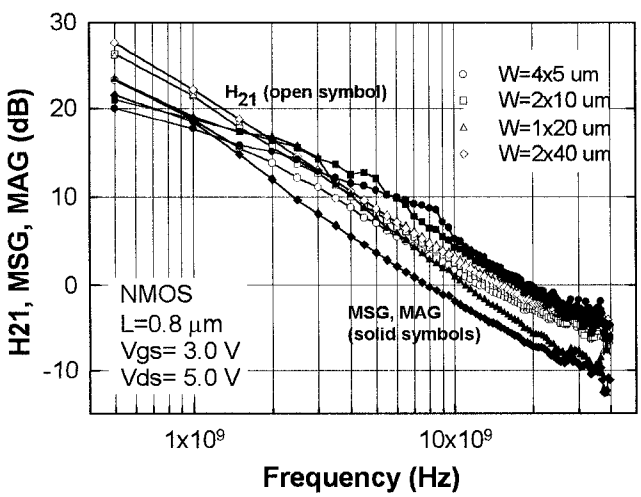

Fig. 2. Measured H_{21} and MAG for 0.8 μm multi-finger nMOSFET. (Unit finger width 40, 20, 10, and 5 μm)

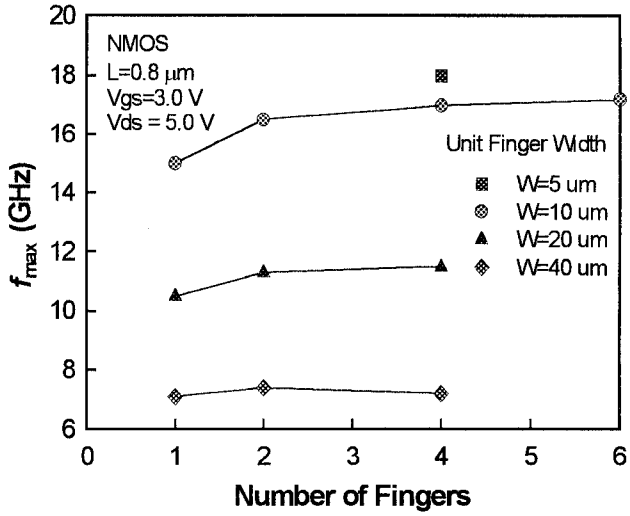

Fig. 3. Measured f_{max} for nMOSFET vs. number of gate finger with several gate width at Vds=5.0V and Vgs=3.0V.

In Fig. 3, the value of f_{max} increases with reducing W_U, but the rate of the f_{max} increase decreases for 5 μm of W_U because the $G_{ds}R_{in}$ term in Eq. (1) becomes dominant. Therefore, W_U of 10 μm seems to be the optimal width to obtain the good RF performance for 0.8 μm polysilicon gate MOSFETs as shown in Fig. 3.

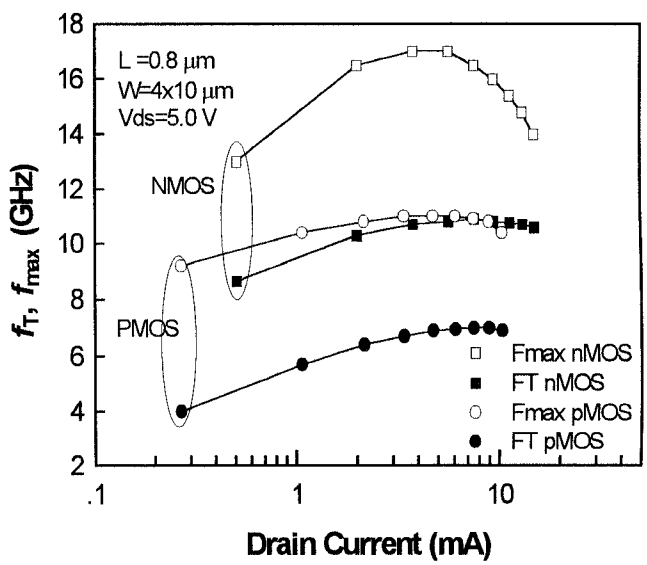

Fig. 4. Measured f_T and f_{max} for n and pMOSFET vs. drain current at Vds=5.0 V.(Vgs=1.0, 1.5, 2.0, 2.5, 3.0, 3.5, 4.0, 4.5, and 5.0 V)

2) Bias Effect on f_T and f_{max}

Fig. 4 shows measured f_T and f_{max} as a function of drain current. Maximum f_{max} of n and pMOSFET was obtained at Vgs=2.5 V (I_D=5.4 mA) and Vgs=3.5 V (I_D= 6.1 mA), respectively. For low power application, the reduction of gate voltage may be performed without the significant performance degradation as shown in this figure.

3) High Frequency Noise Performance

The minimum noise figure F_{min} for MESFET is related to device parameters as follows [5]:

$$F_{min} = 1 + K_2 \, f \, C_{gs} \sqrt{\frac{(R_g + R_s)}{g_m}} \qquad (2)$$

where C_{gs} is the source to gate capacitance, f is the frequency, K_2 is the constant, R_g is the gate resistance, R_s is the source resistance, and g_m is the transconductance. Our measurement results agree well with Eg. (2). F_{min} is directly proportion to frequency at fixed bias as shown in Fig. 5, and the slope of these lines is related to the transconductance depending on gate bias.

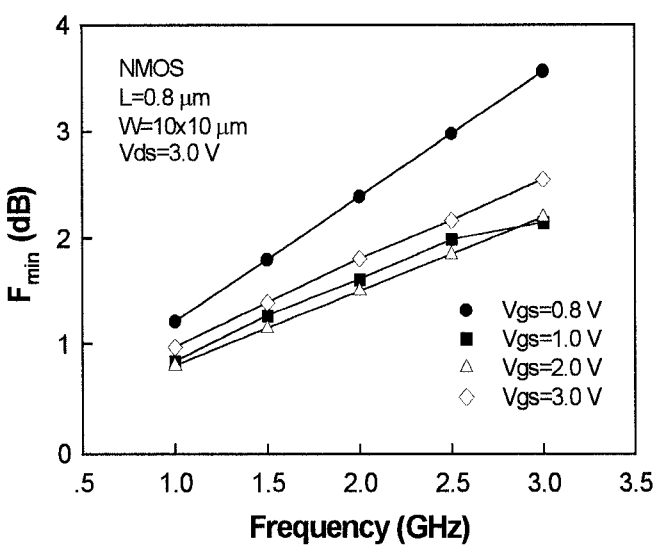

Fig. 5. Measured F_{min} of nMOSFET vs. frequency at several gate bias condition.

Minimum Noise Figure of nMOSFET with the channel width of 4x10 µm was measured at several Vds and Vgs conditions. Using these results, the contour plot of F_{min} at the frequency of 2 GHz is generated in Fig. 6. At Vds=3.0 V and Vgs=2.0 V, which is the bias condition for maximum g_m, F_{min} of nMOSFET becomes the minimum value of 2.0 dB. This result is well consistent with the fact that F_{min} and noise resistance (R_n) are inversely proportion to the g_m of device [6].

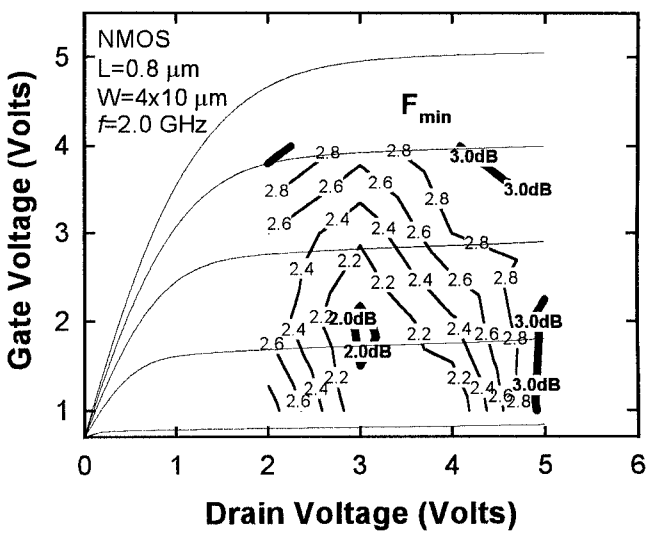

Fig. 6. Contour plot of F_{min} of nMOSFET measured at the saturation bias condition with the frequency of 2 GHz.

4) Performance of Large Width Device for Low Noise Amplifier (LNA)

For low noise applications, a large width device is needed to obtain high g_m. To increase the value of g_m under the optimized W_U and bias condition obtained above, the various devices with large widths of 100, 200, and 600 µm were used. Fig. 7 shows the plot of F_{min} and associate gain vs. drain current with varying the width of devices. The F_{min} of nMOSFET (W=600 µm) was found to be 0.91 dB at 2 GHz with the associated gain of 12 dB. If design specifications of gain, noise, and power for RF amplifiers are given, Fig. 7 will be useful guide information. For the low-noise matching, R_n should be small enough to make noise figure of a MOSFET circuit less sensitive to source impedance

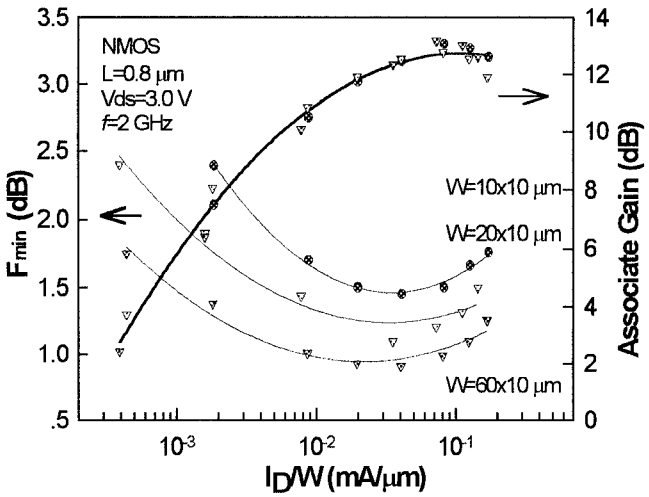

Fig. 7. F_{min} and associate gain vs. I_D/W for large width nMOSFET at Vds=3.0 V.

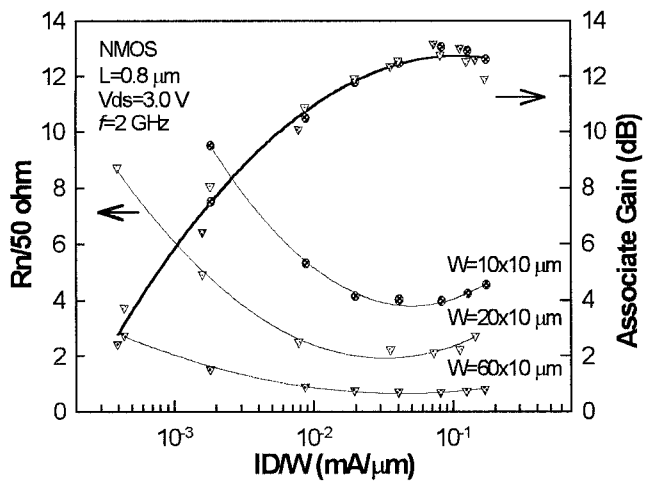

Fig. 8. Noise Resistance vs. I_D/W for large width nMOSFET at Vds=3.0 V.

mismatch [7]. To reduce R_n down to 50 Ω, the channel width of 600 μm is needed in our 0.8 μm nMOSFET as shown in Fig. 8. These results confirm that 0.8 μm nMOSFET is a good candidate for LNA and other RF ICs in the frequency range of 1~2 GHz.

Spiral inductors with the metal thickness of 1.1 μm fabricated on high resistivity Si substrate shows inductance of 3~35 nH with the variation of geometry[8].

Two stage cascade type LNA with the on chip spiral inductor which is used for series feedback and input/output impedance matching was designed at 2 GHz. Simulated results show that gain of 16.9 dB and noise figure of 3.1 dB were obtained at 2 GHz.

CONCLUSIONS

RF and noise performances of 0.8 μm CMOS device have been analyzed to find the optimal layout and bias condition. NMOSFET with the width of 4x10 μm at the bias condition of Vds=3.0 V and Vgs=2.0 V was found to be the highest f_{max} and lowest F_{min}. At the conditions, F_{min} of 0.91 dB with the associated gain of 12 dB was obtained with the large width nMOSFET (W=600 μm), and the simulation for low noise amplifier is also performed for RF IC applications. The 0.8 μm CMOS process provides the possibility of integrating RF front-end modules in a single chip MMIC with low cost.

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